CU1-CHORUS

CompactPCI® Intelligent 16-Port Universal Asynchronous Serial Adapter

User's Manual

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About this Manual

This manual describes the technical aspects of the CU1-CHORUS, required for installation and system integration. It is intended for the experienced user only.

Edition History

EKF Document	Ed.	Contents/*Changes*	Author	Date
Text # 2326 cu1mle.wpd	3	3. Edition User Manual CU1-CHORUS English	gn	March 2000
	4	Added chapter “About this Manual”, set header font size to 12pt, set footer font to Arial, removed all hints to access I/O devices in passive i960 mode.	gn	2. April 2001
	5	Reformatted section ‘Introduction and Overview’, added photographic images CU9-BASE, added circuitry block diagram, replaced component assembly drawing, ocurrences of P1 P4 P5 changed to J1 J4 J5, added section ‘Rear-I/O Module’, changed table ‘Ordering Information’	jj	May 21, 2001

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Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

i960 RP: ® Intel
CompactPCI : ® PICMG
Windows 98, Windows NT, Windows 2000: ® Microsoft

EKF does not claim this list to be complete.

Legal Exclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

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Introduction and Overview

Despite emerging communication standards like FireWire, Fibre Channel or Gigabit-Ethernet: the most common data interface in use is the RS-232 (asynchronous serial interface).

Most industrial computer systems however (in this manner comparable to their office desktop companions) are limited to 2 serial ports, sometimes charged already by peripherals like mouse and modem. In addition, the typical COM ports are generating considerable interrupt load when operated with higher Baudrates, hence reducing noticeable the host CPU performance.

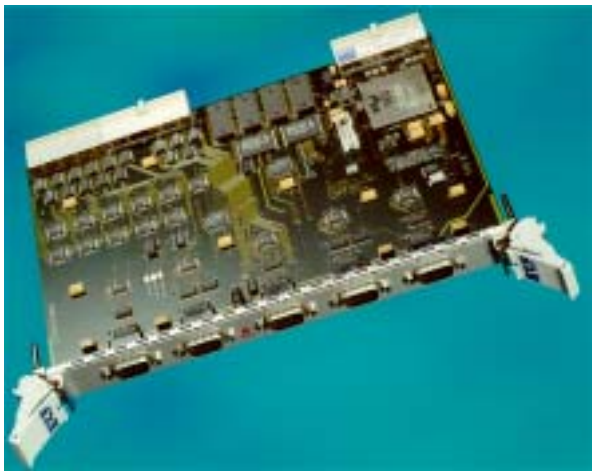
The solution to these problems is a multi-port UART interface board with local intelligence for preprocessing and buffering the serial data streams.

The intelligent ***CompactPCI®*** hostadapter CU1-CHORUS provides a total of 16 serial ports (16550 type UARTs), each capable of bitrates up to 230.4kbps.

Equipped with the powerful embedded processor i960RP(D), the board profits from the built-in PCI bridge as interface to the ***CompactPCI®*** system bus. 8MB DRAM and 4MB Flash EEPROM offer generous local data buffering and program space.

The serial ports are configured as RS-232, or any other standard (e.g. RS-485) by means of an additionally available rear I/O transition board and PHY interface modules.

Hence the CU1-CHORUS is ideally suited for all hard real-time applications with demand for serial interfaces, e.g. data acquisition, data concentration and machine control.



CU1-CHORUS

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Five of the serial ports are ready to use RS-232 configured, reachable by the corresponding 9-pin D-Sub connectors protruding through the front panel of the CU1-CHORUS. In addition, all 16 UART channels are wired as TTL-level signals to the rear connectors J4/J5. By employing external transition modules with built-in transceivers, not only the RS-232, but also any other popular industrial standard as RS-422/485 can be realized, including isolated interfaces.

The CU1-CHORUS hardware supports the I_2O interface. This is a layered, standardized driver concept, modelled after the OSI reference, suitable especially for intelligent I/O sub-processors.

The EKF drivers treat the CU1-CHORUS module as 16C550 compatible COM ports. The drivers allow arbitrary names e.g. COM3..COM18 to be associated with the ports of a CHORUS.

Developers might prefer to collect serial data for block transfers or local preprocessing directly on the CHORUS board. Program and data can be stored in a generous amount of local memory (8MB DRAM and 4MB Flash EEPROM). As a development tool, EKF provides the resident monitor/debugger MON960, which allows stand-alone operation and download of programs via CPCI bus or serial interface. Furthermore EKF can offer turn key ready application programming support.

Use of the CU1-CHORUS frees the host-CPU from critical low level tasks, an essential criterion for real-time applications. Because the CHORUS can be supplemented by a variety of external transition (transceiver) modules for popular serial interface standards, it is a smart and flexible solution to many different industrial applications, offering a fast time to market at moderate cost.

CU1-CHORUS with Rear-I/O Module

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Handling Information

Precautions

This *CompactPCI* ® board contains **electrostatic sensitive** devices. The board should therefore remain in its original EKF packaging until it is used. The antistatic coated film and box provide double protection against electromagnetic discharging as well as against dust, corrosion and mechanical damaging. Be sure to equalize the electrical potential of the board and the *CompactPCI* ® rack before taking out the board of the packaging (by touching the packaging and metallic parts of the rack at the same time, or better by wearing a ground strap). Please keep the original packaging for the case of return. Notice that installing or removing of boards or other system components may done only by authorized persons.

Guidelines to EMC Protection

To fulfill the **CE** specifications with regard to **EMC** take notice of the following guidelines:

- Installation and operation only in EMC systems.
- Close unused system slots with dummy panels.
- Close unused front elements (e.g. RS-232 interfaces) with metallic caps.
- Use shielded cables only.
- Use ferrites to prevent electromagnetic interference (EMI).
- Protect sensible interfaces (e.g. Cheapernet) with plastic caps.

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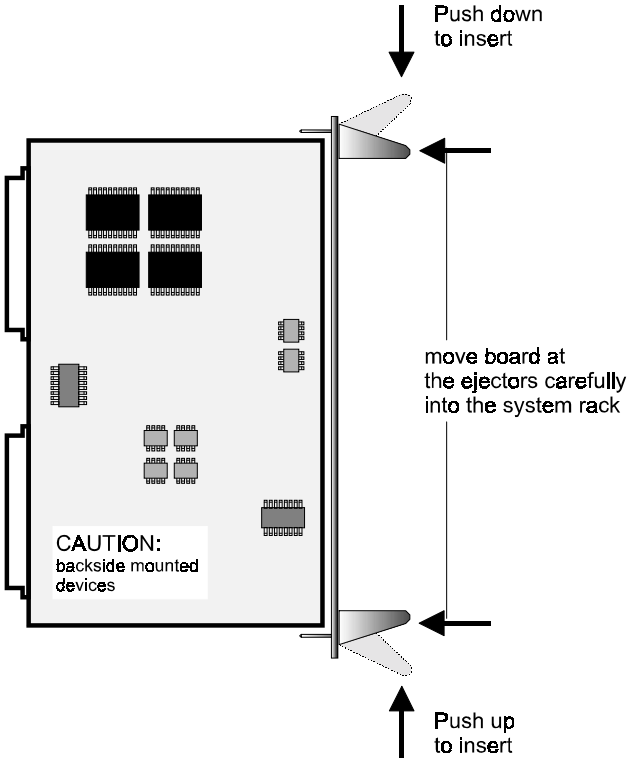
Installing boards

- Switch off the main power supply.
- Touch the system rack to guarantee electrostatic discharge.
- Move board carefully along the guide rails in the chosen slot of the rack. Caution is given especially to the devices mounted on the backside of the circuit board.
- Press the *CompactPCI* ® connectors of the board into the backplane receptacles by pushing the ejectors in the front panel together (see illustration below).
- Optionally screw board and rack together.
- Switch on the main power supply.



Installing board into the system rack

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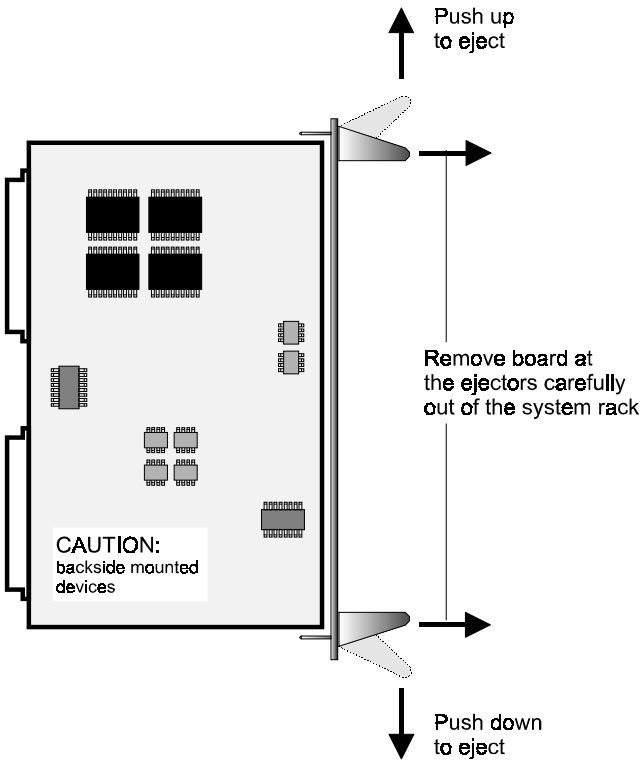
Removing boards

- Switch off the main power supply.
- Touch the system rack to guarantee electrostatic discharge.
- Optionally remove screws if board and rack are mounted together.
- Press the board out of the *CompactPCI* ® backplane by pushing the ejectors in the front panel apart each other (see illustration below).
- Move board carefully along the guide rails out of the rack. Caution is given especially to the devices mounted on the backside of the circuit board.
- Put the removed board in the original EKF packaging box.



Removing board from the system rack

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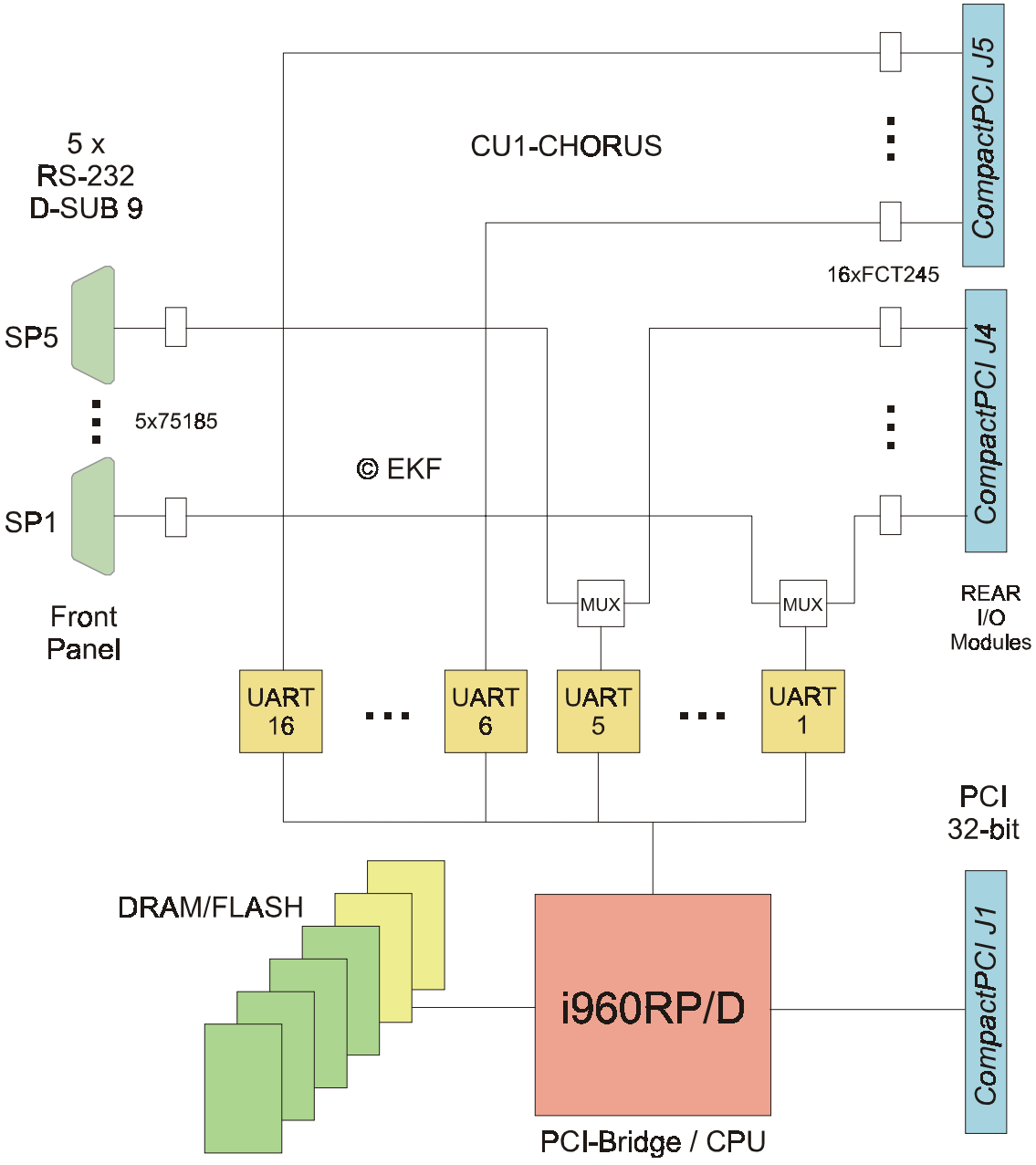
Block Diagram CU1-CHORUS



Block Diagram CU1-CHORUS

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Connectors, Jumper Fields, Factory Defaults

CU1-CHORUS • Component Assembly Drawing

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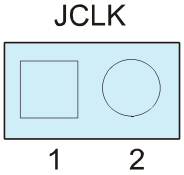
Connectors

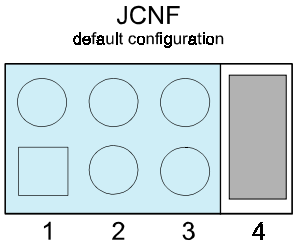
JACCBUS	ACCESS.bus / I^2C Interface (4-pin Header)
J1	*CompactPCI* ® Connector
J4	*CompactPCI* ® Connector (serial I/O Port 1 - 5)
J5	*CompactPCI* ® Connector (serial I/O Port 6 - 16)
SP1 - SP5	RS-232 Serial Interfaces (D-Sub 9)

Jumper Field Factory Defaults



Factory Default
JCLK

Clock Source Selector:
Clock sourced from *CompactPCI* ® Bus Clock



Factory Default **JCNF**

i960®RP Configuration Selector:

1. Initialization Mode 3 (CPU starts after reset)
2. Retry CPCI Configuration Cycles
3. BIST active
4. CPCI Reset Passed Through to Local Reset

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i960®RP Processor

General Features

The central unit on the CU1-CHORUS is an i960®RP I/O Processor, a member of the 80960 family of high performance processors. It combines a high-speed CPU with powerful features to create an intelligent I/O processor and integrates it into a Peripheral Components Interconnect (PCI) environment. This multi-function PCI device is fully compliant with the *PCI Local Bus Specification*, revision 2.1. The i960®RP local bus, a 32-bit multiplexed burst bus, is a high-speed interface to system memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs). The core can maintain a sustained execution rate of one instruction per clock of most instructions.

The i960®RP features include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way, integrated instruction cache
- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated, zero wait state data RAM
- PCI-to-PCI Bridge Unit
- Address Translation Unit
- DMA Controller
- Messaging Unit
- Memory Controller
- I^2C Bus Interface Unit

The Address Translation Unit (ATU) permits direct data access from the ***CompactPCI*** ® interface to local memory. This allows for example the programming of the FLASH devices or downloading software to local memory via the primary *CompactPCI* ® interface without interaction of the i960®RP core. Address translation is controlled through programmable, memory-mapped registers accessible from both the PCI interface and the i960 core processor. The primary ATU has a dedicated PCI configuration space that is accessible through the *CompactPCI* ® bus or the i960 core.

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and i960®RP local memory. Three separate DMA channels accommodate data transfers: two for the *CompactPCI* ® bus, one for the secondary PCI bus (not usable on the CU1-CHORUS). The DMA Controller supports chaining and unaligned data transfers.

The Messaging Unit (MU) provides data transfer between the PCI system and the i960®RP. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues and Index Registers. Each allows a host processor or external PCI device and the i960®RP to communicate through message passing and interrupt generation. The MU makes it easy to realize the Intelligent I/O Interface I_2O.

The Memory Controller allows direct control of the external memory respectively the memory-mapped I/Os on the CU1-CHORUS, including DRAM and Flash EEPROM. It features programmable chip selects and a wait state generator. External memory can be configured as PCI addressable memory or private i960®RP memory.

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Since there is no need for it, the secondary PCI interface of the i960®RP is unconnected on the CU1-CHORUS. Therefore it wether makes sense to use the PCI-to-PCI Bridge unit nor the secondary ATU.

Additional Documentation

A detailed description of these and other features including the programming of the i960®RP processor could be find in the documentation listed below. Electronic information can be obtained via

http://www.intel.com

i960®RP Related Documentation

Document Title	Order Number
i960®Rx I/O Microprocessor Developer's Manual	Intel Order # 272736
i960®Rx I/O Processor Specification Update	Intel Order # 272918
i960®RP/RD I/O Processor at 3.3 Volts data sheet	Intel Order # 273001
i960®Jx Microprocessor User's Guide	Intel Order # 272483

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Clock and Reset Generation

Clock Generation

The CU1-CHORUS is clocked by a single, 33 MHz signal. This master clock controls the entire timing of the i960®RP. The main clock input is fed by one of two possible sources, chosen by the 2x1 clock selection jumper **JCLK** near the **J1** connector on the CU1-CHORUS:

Clock Selection Jumper JCLK Setting Options

Clock Source	JCLK
CompactPCI ® Bus Clock Signal (**J1** Pin D6)	removed
33 MHz Oscillator on the CU1-CHORUS	set

Normally the CU1-CHORUS will be integrated in a *CompactPCI* ® rack with a system controller and possibly other boards. In this case always the bus clock signal should be used as clock source (**JCLK** removed!).

To support a single stand-alone operation without system controller the CU1-CHORUS provides an on-board 33 MHz oscillator that generates the necessary clock. When setting the jumper **JCLK** the oscillators output is connected to the clock input of the board.

CAUTION:
Note that in this case the clock signal also occurs on the clock pin of the *CompactPCI* ® connector **J1** (Pin D6). This will lead to clock signal crashing on the bus if more than one board drives the clock.

The clock signal is distributed on the CU1-CHORUS via a dedicated clock buffer to provide a low skew, well conditioned signal as required by the PCI specification.

Power-On and Manual Reset

There are a lot of reasons which trigger a reset on the CU1-CHORUS:

(1) Power-On (switching on the power supply)
(2) V_{cc5} drops below 4.65V (power failed)
(3) V_{cc3} drops below 3.0V (power failed)
(4) Pushing the **RESET** Push Button in the front panel
(5) Triggering the *CompactPCI* ® reset signal (**J1** Pin C5, **JCNF**(4) on)
(6) Reaching time out of the hardware watchdog
(7) Software reset caused by the i960®RP processor

The first 6 sources will reset all devices on the CU1-CHORUS to a known state. An integrated power supervisor generates a clean reset signal with a minimum length of 140 ms even if the

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voltages haven't stabilized at power-on. The signal is fed to the i960®RP, the Flash EEPROMs and the serial controllers 16C550. The processor can reset all the 16C550s by triggering the local bus reset signal in the Extended Bridge Control Register (EBCR, bit 5).

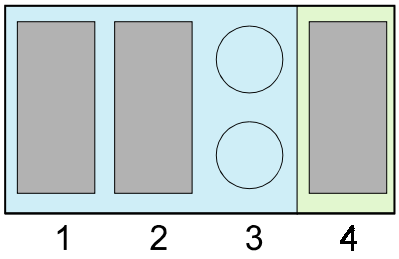
Hardware Watchdog

The CU1-CHORUS is equipped with a hardware watchdog. The watchdog is disabled after a hardware reset. It is activated by toggling the general purpose output OUT1# of port 1's UART. This is done by changing bit 2 in the Modem Control Register MCR of the UART (see section *Serial Controller 16C550* for details of the UART's registers).

If the processor once touched MCR(2), the watchdog is armed and must be triggered at least every 1000 ms. A hardware reset will occur after a maximum time of 1.6 sec after the last watchdog trigger pulse.

i960®RP Initialization Modes

The behavior of the i960®RP after reset is controlled by the configuration selection jumper field JCNF. The processor supports four initialization modes 0 to 3, where mode 1 makes no sense on the CU1-CHORUS.



Jumper Field JCNF

Configuration Jumper Field JCNF Initialization Mode Setting Options

Initialization Mode	JCNF 1	JCNF 2	*CompactPCI* ® Interface	i960RP core processor
Mode 0	set	set	accepts transactions	held in reset
Mode 1 [1])	set	removed	retries all config. transactions	held in reset
Mode 2	removed	set	accepts transactions	initializes
Mode 3	removed	removed	retries all config. transactions	initializes

[1]) Not useful on the CU1-CHORUS

Mode 0 allows a host processor to configure the i960®RP peripherals while the i960 core processor is held in reset. The host processor configures the PCI-to-PCI bridge by assigning bus

numbers, allocating PCI address space, and assigning IRQ numbers. The memory controller and ATU can also be initialized by the host processor. Program code for the i960 core processor may be downloaded into local DRAM or Flash EEPROM by the host processor. The host processor then clears the i960 reset signal by clearing the Core Processor Reset bit in the Extended Bridge Control Register (EBCR, bit 1). This deasserts the internal reset signal on the i960 core processor and the processor begins its initialization process.

Mode 2 allows configuration cycles on the PCI-to-PCI bridge at any time and allows the i960 core processor to initialize after reset. Mode 2 allows each unit of the i960®RP to be initialized in its own manner. Be aware that race conditions may exist between i960 core operation after reset and host processor PCI configuration.

Mode 3 allows the i960 core processor to initialize and control the initialization process before the host processor is allowed to configure the i960®RP peripherals. During this time, the *CompactPCI* ® interface signals a Retry on all configuration cycles it receives until the i960 core processor clears the Configuration Cycle Disable bit in the EBCR.

The 3rd jumper of JCNF exists to enable or disable the i960®RP's build-in self test (BIST). If enabled the processor tries to check all its internal units. If the check failed the processor asserts a signal that lights the red on-board LED CPU FAIL and core execution stops. Because BIST needs about 414000 CPU cycles it may be necessary to disable it when the restart time needs to be minimized.

Configuration Jumper Field JCNF BIST Setting Options

JCNF 3	Processor BIST
removed	enabled
set	disabled

Jumper 4 of JCNF is used to forward the reset signal from the *CompactPCI* ® bus to the CPU and the other local devices on the board.

Configuration Jumper Field JCNF CPCI Reset Setting Options

JCNF 4	CPCI Reset
removed	ignored
set	forwarded to the board

It is a good idea to remove JCNF 4 when the BIOS of the main CPU board within the *CompactPCI* ® does not recognize the CU1-CHORUS after system reset.

Local Memory Devices

Flash EEPROM

The CU1-CHORUS is equipped with on-board programmable Flash EEPROM devices. The data bus width to these devices is 32-bit allowing the i960®RP to execute program code from Flash in full speed. Therefore it is not necessary to copy the code into DRAM. The Flash devices are connected to the memory bank 0 of the i960®RP Memory Controller. They are readable and especially writeable any time with no need to enable the programming voltage. Caution is given when the processor itself tries to program the Flash devices while executing code from the Flashs. This will lead to a hanging processor core. To program the Flash devices use one of the following alternates:

1. Programming by i960®RP core processor: Copy the program data and the Flash programming algorithm code to DRAM. Run the programming code from DRAM. Return to the calling function or restart the code loaded into the Flash devices.

2. Programming via *CompactPCI* ® interface: Reset the CU1-CHORUS with JCNF setting to initialization mode 0. Alternatively the i960®RP core processor could be halted by executing the HALT instruction. Program the Flash devices via the primary ATU. Restart the processor.

Depending on the version of the CU1-CHORUS there are different types of Flash devices in use:

- 28F016SV / Intel
- 28F160S5 / Intel

These devices distinguish in access times and programming algorithms. Programming tools (currently running on LINUX or WinXX) are offered by EKF and are available on request. The following table shows the necessary initializations in the read and write wait state registers (MBRWS0, MBWWS0) of the i960®RP memory controller dependent on the devices in use. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

Flash Device Read And Write Wait State Settings

Flash Device	Read		Write	
	Access [ns]	MBRWS0	Access [ns]	MBWWS0
28F016SV	70	0x00000220	70	0x00000221
28F160S5	70	0x00000220	70	0x00000220

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Dynamic Random Access Memory (DRAM)

The CU1-CHORUS offers a working memory space of 8 Mbyte. The memory is organized in two banks of non-interleaved DRAM, each 4 Mbyte in size. The data path width is 32-bit without parity. Similar to the Flash EEPROMs different types of DRAM devices are in use. Possible types are

- Fast Page Mode (FPM) DRAMs
- Extended Data Out (EDO) DRAMs

with an access time of at least 70 ns. The following table shows typical values to program to the i960®RP memory controller to setup the DRAM interface. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

DRAM Initialization Parameters

Name	Register	Value	Description
DRWS	DRAM Bank Read Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DWWS	DRAM Bank Write Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DRIR	DRAM Refresh Interval	0x00010204	Refresh enabled, 15.625 µs refresh interval
DPER	DRAM Parity Enable	0x00000000	DRAM parity disabled
DBCR	DRAM Bank Control	0x0000000D 0x0000004D	High-current drives disabled, DRAM bank enables, Fast Page Mode (FPM), 2 banks or Extended Data Out (EDO), 2 banks

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I^2C Interface

The i960®RP supports a master and slave interface to the popular I^2C (Inter-Integrated Circuit) bus. This simple, two wire serial bus allows an easy connection to other I^2C devices. Transfer rates of up to 400 Kbit/s are possible. It could be programmed via the I^2C unit registers of the i960®RP.

An I^2C message consists of a device addressing byte and additional data bytes. The device address byte also contains the information wether the following operations are read or write transfers. If the address of an I^2C slave device on the bus matches the device address byte sent by a master, the slave acknowledges the transfer.

General I^2C Addressing Byte Format

A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W
MSB							LSB

On write operations (R/W=0) the master may send then further data bytes to the slave until the master generates a stop condition. Each byte transferred is acknowledged by the recipient. Read operations are working in the same way except that R/W=1 and that the data flow is reversed.

Serial EEPROM 24C32

The CU1-CHORUS offers a serial EEPROM 24C32 with a capacity of 4 Kbytes. This device can be used e.g. to permanently store important parameters that should be non volatile even if the power disappears. It is accessible as slave device via the I^2C bus. Write accesses to the memory array of the serial EEPROM are possible any time because the hardware write protection feature of the 24C32 is not enabled on CU1-CHORUS.

Serial EEPROM 24C32 Addressing Byte Format

1	0	1	0	0	0	0	R/W
MSB				A_2	A_1	A_0	LSB

The above figure shows the I^2C bus device addressing byte that must be written to the serial EEPROM in order to read (R/W=1: DeviceAddr=0xA1) or write (R/W=0: DeviceAddr=0xA0) data from or to it (the 3 external address lines A_{2-0} offered by the 24C32 are hard-wired to GND on the CU1-CHORUS). Read and write accesses with the I^2C bus maximum speed of 400 Kbit/s are supported by the device.

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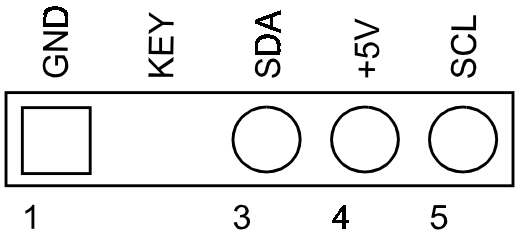
ACCESS.bus Interface

To make it easy to connect external I^2C devices to the CU1-CHORUS the board offers an ACCESS.bus interface via the 4-pin connector **JACCBUS**. The ACCESS.bus is similar to the System Management Bus (SMBus) based on the I^2C bus. Both standards are compatible to the I^2C bus with exception of a few electrically (e.g. max. load capacity) and mechanical (e.g. ACCESS.bus defines a connector, I^2C does not) specifications.

The ACCESS.bus interface on the CU1-CHORUS supports up to 126 devices (7-bit device addresses minus the broadcast address and the on-board serial EEPROM) over a total cable length of 8 m with a maximum data rate of 100 Kbit/s. Each device may use its own data rate. The cable consists of two shielded pairs: a Ground/+5V pair and a clock/data pair.



Connector **JACCBUS**

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Serial Interfaces

The CU1-CHORUS offers sixteen serial interfaces. The signals of these ports are fed to different connectors on the board. The first 5 ports are wired as RS-232 interfaces to the 5 male D-Sub 9 connectors in the front panel of the board labeled as **SP1** - **SP5**. This allows to make simple links to serial interfaces of terminals, personal computers, modems etc. with usual cables.

In addition all sixteen interfaces are available on the *CompactPCI* ® connectors J4 and J5. Each serial port could be connected to a transition module, which allows the conversion to different physical interface standards like RS-232, RS-422, RS-485, with or without optical isolation.

Serial Controller 16C550

The serial interfaces are based on the well known Asynchronous Communication Element (ACE) 16C550. These UARTs are clocked with a separate 14.7456 MHz oscillator leading to transfer rates of up to 921.6 KBaud. Due to the fact that the 16C550 could be clocked up to 16 MHz, higher baud rates are also possible by using an accordingly oscillator (deliverable on request).

The next table shows the transmission bit rates, the value of the UART's divisor latch register (iDiv) and the resulting baud rate errors in dependency of the clock in use:

UART Data Transmission Bit-Rates

Clock	Baud	Divisor	iDiv	Error
14745600	75	12288.0	12288	0.00%
14745600	110	8378.2	8378	0.00%
14745600	135	6826.7	6827	0.00%
14745600	150	6144.0	6144	0.00%
14745600	300	3072.0	3072	0.00%
14745600	600	1536.0	1536	0.00%
14745600	1200	768.0	768	0.00%
14745600	1800	512.0	512	0.00%
14745600	2400	384.0	384	0.00%
14745600	4800	192.0	192	0.00%
14745600	7200	128.0	128	0.00%
14745600	9600	96.0	96	0.00%
14745600	14400	64.0	64	0.00%
14745600	19200	48.0	48	0.00%
14745600	38400	24.0	24	0.00%
14745600	56000	16.5	16	-2.78%

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Clock	Baud	Divisor	iDiv	Error
14745600	57600	16.0	16	0.00%
14745600	115200	8.0	8	0.00%
14745600	128000	7.2	7	-2.78%
14745600	230400	4	4	0.00%
14745600	460800	2	2	0.00%
14745600	921600	1	1	0.00%
16000000	75	13333.3	13333	0.00%
16000000	110	9090.9	9091	0.00%
16000000	135	7407.4	7407	-0.01%
16000000	150	6666.7	6667	+0.01%
16000000	300	3333.3	3333	-0.01%
16000000	600	1666.7	1667	+0.02%
16000000	1200	833.3	833	-0.04%
16000000	1800	555.6	556	+0.08%
16000000	2400	416.7	417	+0.08%
16000000	4800	208.3	208	-0.16%
16000000	7200	138.9	139	+0.08%
16000000	9600	104.2	104	-0.16%
16000000	14400	69.4	69	-0.64%
16000000	19200	52.1	52	-0.16%
16000000	38400	26.0	26	-0.16%
16000000	56000	17.9	18	+0.80%
16000000	57600	17.4	17	-2.08%
16000000	115200	8.7	9	+3.68%
16000000	125000	8	8	0.00%
16000000	128000	7,8	8	+2.40%
16000000	250000	4	4	0.00%
16000000	500000	2	2	0.00%
16000000	1000000	1	1	0.00%

The UARTs are connected to bank 1 of the i960®RP's memory controller. The following table shows the addressing of the registers of the 1st UART relative to its base address:

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UART (16C550) Register Offset Definitions

Base Address Offset	Read Access	Write Access
0x00	Receiver Buffer Register (**RBR**)	Transmitter Holding Register (**THR**)
0x04	Interrupt Enable Register (**IER**)	Interrupt Enable Register (**IER**)
0x08	Interrupt Ident. Register (**IIR**)	FIFO Control Register (**FCR**)
0x0C	Line Control Register (**LCR**)	Line Control Register (**LCR**)
0x10	Modem Control Register (**MCR**)	Modem Control Register (**MCR**)
0x14	Line Status Register (**LSR**)	not allowed
0x18	Modem Status Register (**MSR**)	ignored
0x1C	Scratch Register (**SCR**)	Scratch Register (**SCR**)

The 1st register of the UART of the 2nd port starts at relative address 0x20, the UART of the 3rd port at address 0x40 and so on.

UART (16C550) Port Offset Definitions

Port Number	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Base Address Offset	0x00	0x20	0x40	0x60	0x80	0xA0	0xC0	0xE0
Port Number	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Base Address Offset	0x100	0x120	0x140	0x160	0x180	0x1A0	0x1C0	0x1E0

In order to get a proper function of the UARTs, the following values should be programmed to the wait state registers of memory bank 1. Burst accesses to the UARTs are not allowed.

UART (16C550) Read And Write Wait State Settings

MBRWS1	MBWWS1
0x00000302	0x00000302

The UARTs are able to request i960®RP core interrupts. On the CU1-CHORUS are two interrupt modes available:

(1) Collected Interrupt Mode: The request lines of all the UARTs are pulled together to the interrupt input XINT0# of the processor (default mode after reset).
(2) Distributed Interrupt Mode: The request lines of the UARTs are fed to XINT0# - XINT7# of the processor.

The interrupt mode is chosen by the general purpose output OUT2# of the 1st UART. This port can be switched by accessing bit 3 of the Modem Control Register MCR:

Interrupt Mode Selection

Interrupt Mode	MCR(3)
Collected Interrupt Mode (default after reset)	0
Distributed Interrupt Mode	1

Distributed Interrupt Mode Request Pin Table

Port Number	1	2	3	4	5	6	7	8
Port Number	9	10	11	12	13	14	15	16
Interrupt Request Pin	XINT0#	XINT1#	XINT2#	XINT3#	XINT4#	XINT5#	XINT6#	XINT7#

An IRQ can be identified by checking the IIR of the UART in the interrupt service routine. The request is released by accessing the corresponding register that caused the interrupt (e.g. reading an incoming character from the RBR). See UART data sheets and i960®RP manual for detailed description of interrupt programming.

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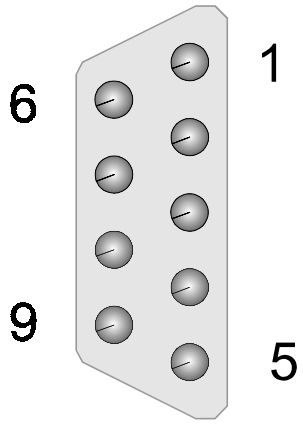
Connectors SP1 - SP5 (RS-232)

The illustration below shows the pin assignments to the connectors **SP1 - SP5** (front view of the connectors). Signal directions are seen from the view of the CU1-CHORUS, e.g. **RXD** (**SP1**, pin 2) is an input to the CU1-CHORUS.



Male D-Sub 9 Connector (PC compatible)

SP1 - SP5 (RS-232E/V.28)		
	1	DCD
DSR	6	
	2	RXD
RTS	7	
	3	TXD
CTS	8	
	4	DTR
RI	9	
	5	GND

CAUTION: If one of the ports **SP1 - SP5** is used do not connect to any signal of the same port on *CompactPCI* ® connector **J4**. Each port is usable only once.

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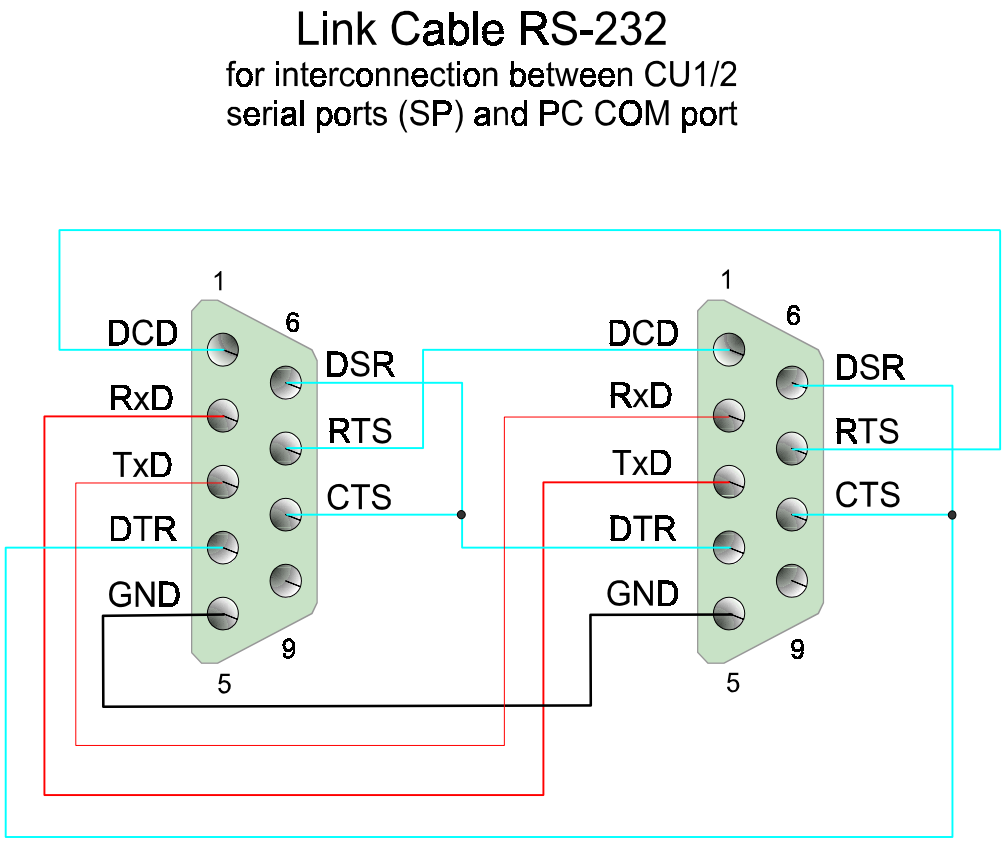
The following figure shows the wiring scheme of a standard RS-232 link cable usually in use to connect a port of the CU1-CHORUS with another RS-232 port, e.g. a COM port of a PC:



Link Cable RS-232

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Serial Interfaces on J4/J5

To allow a maximum flexibility the CU1-CHORUS offers an interface to external transition modules via the *CompactPCI* ® connectors **J4** and **J5**. The signals of the first 5 serial interfaces are connected to **J4**, ports 6 to 16 are connected to **J5**. The splitting of the ports in this way makes it possible to let the **J4** unmounted (e.g. when using the CU1-CHORUS in the *CompactPCI* ® Computer Telephony environment H.110) and nevertheless to access the ports 1 - 5 via the front panel connectors.

The transition modules are connected via flat cables and an adapter board to the CU1-CHORUS. See chapter *Ordering Information* for additional information about this stuff.

The following table shows the wiring scheme of the ports on **J4** and **J5**.

CompactPCI Connector J4 Pin Assignment

#J4	A	B	C	D	E
25	NC	NC	NC	NC	NC
24	NC	NC	NC	NC	NC
23	NC	NC	NC	NC	NC
22	NC	NC	NC	NC	NC
21	NC	NC	NC	NC	NC
20	NC	NC	NC	NC	NC
19	NC	NC	NC	NC	NC
18	NC	NC	NC	NC	NC
17	NC	NC	NC	NC	NC
16	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC
14	Coding Key Area (Brilliant Blue)				
13					
12					

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11	NC	NC	NC	NC	NC
10	DSR01#	RXD01	DTR01#	CTS01#	GND
9	5V	RI01#	TXD01	RTS01#	CD01#
8	DSR02#	RXD02	DTR02#	CTS02#	GND
7	5V	RI02#	TXD02	RTS02#	CD02#
6	DSR03#	RXD03	DTR03#	CTS03#	GND
5	5V	RI03#	TXD03	RTS03#	CD03#
4	DSR04#	RXD04	DTR04#	CTS04#	GND
3	5V	RI04#	TXD04	RTS04#	CD04#
2	DSR05#	RXD05	DTR05#	CTS05#	GND
1	5V	RI05#	TXD05	RTS05#	CD05#
#J4	**A**	**B**	**C**	**D**	**E**

CAUTION: If one of the ports SP1 - SP5 is used do not connect to any signal of the same port on *CompactPCI* ® connector J4. Each port is usable only once.

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CompactPCI Connector J5 Pin Assignment

#J5	A	B	C	D	E
22	DSR06#	RXD06	DTR06#	CTS06#	GND
21	5V	RI06#	TXD06	RTS06#	CD06#
20	DSR07#	RXD07	DTR07#	CTS07#	GND
19	5V	RI07#	TXD07	RTS07#	CD07#
18	DSR08#	RXD08	DTR08#	CTS08#	GND
17	5V	RI08#	TXD08	RTS08#	CD08#
16	DSR09#	RXD09	DTR09#	CTS09#	GND
15	5V	RI09#	TXD09	RTS09#	CD09#
14	DSR10#	RXD10	DTR10#	CTS10#	GND
13	5V	RI10#	TXD10	RTS10#	CD10#
12	DSR11#	RXD11	DTR11#	CTS11#	GND
11	5V	RI11#	TXD11	RTS11#	CD11#
10	DSR12#	RXD12	DTR12#	CTS12#	GND
9	5V	RI12#	TXD12	RTS12#	CD12#
8	DSR13#	RXD13	DTR13#	CTS13#	GND
7	5V	RI13#	TXD13	RTS13#	CD13#
6	DSR14#	RXD14	DTR14#	CTS14#	GND
5	5V	RI14#	TXD14	RTS14#	CD14#
4	DSR15#	RXD15	DTR15#	CTS15#	GND
3	5V	RI15#	TXD15	RTS15#	CD15#
2	DSR16#	RXD16	DTR16#	CTS16#	GND
1	5V	RI16#	TXD16	RTS16#	CD16#
#J5	**A**	**B**	**C**	**D**	**E**

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Interrupts

The i960®RP provides an on-chip programmable interrupt controller that allows a flexible, priority level based reaction to internal and external events. The processor uses interrupt vector numbers to enter the interrupt service routine (ISR). This mechanism leads to fast reaction and low interrupt latency. To optimize interrupt performance the vectors can be hold in the i960®RP internal RAM and the ISR can be frozen in the instruction cache. See the i960®RP manual for details.

Internal interrupt events have their origin by the different units within the i960®RP like the I^2C unit, the messaging unit etc. External requests are fed to the processor via 8 maskable (XINT0#...XINT7#) and one non-maskable (NMI#) interrupt inputs. Four bits within the PCI interrupt routing select register (PIRSR) decide for each XINT#-pin wether the interrupt is lead to the i960 core or to the *CompactPCI* ® interface.

The CU1-CHORUS owns the following peripheral interrupt devices:

(1) the serial controllers via XINT0# or XINT0# - XINT7# depending on interrupt mode in use
(2) the NMI push button via NMI# (non-maskable!)

For a description of the serial controller interrupts refer to the corresponding chapter.

The NMI push button is located at the backside of the RESET push button. Since no space was available in the front panel the button is directed toward the board center.

The NMI push button is a nice tool when debugging software on the CU1-CHORUS. A debugger can enter the control of a running program when pushing the NMI push button. Because this interrupt can not be masked by a program, getting program control is always possible. The interrupt request of the NMI button is active while the button is pushed. It can be identified by checking the NMI interrupt status register (NISR, bit 8).

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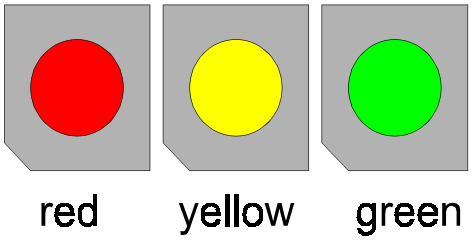
Diagnostics Display

There are three LEDs on the CU1-CHORUS indicating the current state of the board. Since no space was available **in the front panel** the LEDs are mounted near the back side of the **SP1** connector (they are visible only if the *CompactPCI* ® rack is not closed completely).



Diagnostics Display

The LEDs are having to following meaning:

Diagnostics Display Information

LED	lighten	not lighten
red (core state)	build-in self test failed, or local bus confidence test failed, or processor held in reset state: core execution stopped	both build-in self test and local bus confidence test passed: core is in executing mode
yellow (UART access)	access to one of the serial controllers	no access to any of the serial controllers
green (local access)	access to local DRAM, Flash or UARTs	no access to any local device

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CompactPCI ® Interface

The CU1-CHORUS offers a *CompactPCI* ® interface complying to the *CompactPCI* ® *Specification Revision 2.1*. *CompactPCI* ® is an industrial implementation of the familiar *Peripheral Component Interconnect* (PCI) bus. It combines the well known electrical features of PCI with the more robust mechanical 19 inch rack mounting technology. The interface supports 64-bit address and 32-bit data transfers. It is designed for a clock frequency of 33 MHz with a transfer rate of up to 132 Mbyte/s.

PCI Devices

The *CompactPCI* ® interface is realized by the i960® RP processor. It consists of two PCI functions, thus it is a multi-function PCI device. The first function (PCI function 0) is the PCI-to-PCI bridge unit which creates a data path between the primary (the *CompactPCI* ®) and the secondary interface (not used on CU1-CHORUS). PCI function 1 is the primary Address Translation Unit (ATU). This unit allows high-speed accesses from the *CompactPCI* ® interface to the local bus devices like Flash EEPROM or DRAM. Normally a BIOS running on a host system detects these PCI devices at boot time.

Address Translation Unit (ATU)

The Address Translation Unit (ATU) provides an interface between the *CompactPCI* ® bus and the i960 local bus. It consists of two parts: the primary ATU for accesses from *CompactPCI* ® and the secondary ATU for accesses from the secondary PCI bus (not used on the CU1-CHORUS). Data transfers initiated by any PCI bus master to a local bus device are called *inbound* transactions. If the i960 core starts a data access to any PCI bus slave, this is called an *outbound* transfer.

The ATU fulfils both address filtering and address translation. For inbound transactions the ATU uses three registers:

- Inbound ATU Base Register
- Inbound ATU Limit Register
- Inbound ATU Translate Value Register

A PCI address is detected as an inbound transaction by the ATU if

(PCI_Address & Limit_Register) == Base_Register.

The incoming 32-bit PCI_Address is bitwise ANDed with the Limit_Register. When the result matches the Base_Register, the PCI_Address is detected as being within the inbound translation window. This opens a PCI address window from (Base_Register) to (Base_Register + Limit_Register). Once the transaction is claimed, the address must be

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translated from a 32-bit PCI address to a 32-bit local address. For that the incoming PCI_Address is first bitwise ANDed with the bitwise inverse of the Limit_Register. This result is bitwise ORed with the ATU Translate_Value_Register. The result is the 32-bit local address:

Local_Address = (PCI_Address & (~Limit_Register)) | Translate_Value_Register

In addition the ATU provides address detection and translation for i960 core processor-initiated cycles targeted to one of the PCI buses. The ATU supports two different translation modes:

- Address Translation Windows
- Direct Addressing Window

The address translation windows are located from 0x8000 0000 to 0x9001 FFFF within the 32-bit local address space of i960 processor. This range consists of two 128 Mbyte memory windows and two 64 Kbyte I/O windows for the primary and secondary ATU respectively. Each memory window is divided into two areas, 64 Mbyte for 32-bit PCI address cycles and 64 Mbyte for PCI double address cycles (DAC). The type of the PCI transfer is dependent from the area that is hit within the address translation window by the i960 core.

The translation mechanism used is very similar to the algorithm for the inbound transactions described above. For memory and DAC accesses it is

PCI_Address = (Local_Address & 0x03FF FFFF) | Memory_Window_Value_Register

I/O transactions are translated by

PCI_Address = (Local_Address & 0x0000 FFFF) | I/O_Window_Value_Register

In addition the i960®RP provides a direct addressing scheme. This method of outbound PCI transactions is limited to memory transfers and works within the local address range from 0x0000 2000 to 0x7FFF FFFF only. If enabled any access to these locations are forwarded to the PCI bus. Which of the PCI buses are used will be decided by a bit in the ATU control register ATUCR. This register also contains the direct addressing enable bit.

As every PCI device the ATU implements its own configuration space. This space is 256 bytes in size, whereas the first 64 bytes must adhere to a predefined header format. The ATU is programmed on the *CompactPCI* ® interface via type 0 configuration commands to PCI function number one. Besides the i960 core processor can access the configuration space via memory mapped registers at local address 0x1200. Some of the read-only registers can also be written by the i960. The following table shows the configuration header according the *PCI Local Bus Specification*, revision 2.1:

Address Translation Unit Configuration Header Format

Address Translation Unit Configuration Header				Address Offset
ATU Device ID		ATU Vendor ID		0x00
ATU Primary Status		ATU Primary Command		0x04
ATU Class Code			ATU Revision ID	0x08
BIST	Header Type	Latency Timer	Cacheline Size	0x0C
Primary Inbound ATU Base Address				0x10
Reserved				0x14
				0x18
				0x1C
				0x20
				0x24
				0x28
ATU Subsystem ID		ATU Subsystem Vendor ID		0x2C
Expansion ROM Base Address				0x30
Reserved				0x34
				0x38
Max. Latency	Minimum Grant	Interrupt Pin	Interrupt Line	0x3C

The next table shows the i960®RP specific registers of the ATU configuration space.

ATU Extended PCI Configuration Header Format

ATU Extended PCI Configuration Register Space	Address Offset
Primary Inbound ATU Limit Register PIALR	0x40
Primary Inbound ATU Translate Value Register PIATVR	0x44
Secondary Inbound ATU Base Address Register SIABAR	0x48
Secondary Inbound ATU Limit Register SIALR	0x4C
Secondary Inbound ATU Translate Value Register SIATVR	0x50
Primary Outbound Memory Window Value Register POMWVR	0x54
Reserved	0x58
Primary Outbound I/O Window Value Register POIOWVR	0x5C
Primary Outbound DAC Window Value Register PODWVR	0x60

Primary Outbound Upper 64-bit DAC Register POUDR		0x64
Secondary Outbound Memory Window Value Register SOMWVR		0x68
Secondary Outbound I/O Window Value Register SOIOWVR		0x6C
Reserved		0x70
Expansion ROM Base Address Register ERBAR		0x74
Expansion ROM Translate Value Register ERTVR		0x78
Reserved		0x7C
		0x80
		0x84
ATU Configuration Register ATUCR		0x88
Reserved		0x8C
Primary ATU Interrupt Status Register PATUISR		0x90
Secondary ATU Interrupt Status Register SATUISR		0x94
Secondary ATU Status Register	Secondary ATU Commond Register	0x98
Secondary Outbound DAC Window Value Register SODWVR		0x9C
Secondary Outbound Upper 64-bit DAC Register SOUDR		0xA0
Primary Outbound Configuration Cycle Address Register POCCAR		0xA4
Secondary Outbound Configuration Cycle Address Register SOCCAR		0xA8
Primary Outbound Configuration Cycle Data Register POCCDR		0xAC
Secondary Outbound Configuration Cycle Data Register SOCDCR		0xB0
Reserved		0xB4 - 0xFF

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System Connector J1

The *CompactPCI* ® specification defines the usage of shielded, 2 mm-pitch, 5-row connectors on *CompactPCI* ® boards according to IEC 917 and IEC 1076-4-101. The 32-bit PCI interface is implemented via the J1 connector, while the 64-bit option requires the connector P2. Since the CU1-CHORUS has a 32-bit *CompactPCI* ® interface the P2 connector is not necessary and thus not mounted.

The J1 connector also defines the supported signaling voltage ($V_{I/O}$). A coding key in this connector is used to distinguish boards with $V_{I/O}$ = 3.3 V (cadmium yellow key), $V_{I/O}$ = 5 V (brilliant blue key) or both (no key). The CU1-CHORUS is laid out for $V_{I/O}$ = 5 V only and equipped with a blue coding key.

CAUTION:

Do not use the CU1-CHORUS within a 3.3 V *CompactPCI* ® system.

CompactPCI Connector J1 Pin Assignment

#J1	A	B	C	D	E
25	5V	REQ64# [1])	ENUM# [1])	3.3V	5V
24	AD1	5V	VI/O	AD0	ACK64# [1])
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN [2])	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	3.3V	PAR	C/BE1#
17	3.3V	SDONE [1])	SBO# [1])	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	GND	TRDY#
14	Coding Key Area (Brilliant Blue)				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	IDSEL	AD23	GND	AD22
8	AD26	GND	VI/O	AD25	AD24

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7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	3.3V	CLK	AD31
5	BRSVJ1A5 [1])	BRSVJ1B5 [1])	RST#	GND	GNT#
4	BRSVJ1A4 [1])	GND	VI/O	INTP [1])	INTS [1])
3	INTA#	INTB#	INTC#	5V	INTD#
2	TCK	5V	TMS	TDO	TDI
1	5V	-12V	TRST#	+12V	5V
#J1	**A**	**B**	**C**	**D**	**E**

Notes:
[1]) These pin positions are not connected on the CU1-CHORUS.
[2]) This signal is hardwired to GND on the CU1-CHORUS.

I/O Connectors J4 and J5

The CU1-CHORUS uses the *CompactPCI* ® connectors J4 and J5 to pass the serial I/O signals to the rear of the system rack. See Chapter *Serial Interfaces* for details of pin assignments.

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Technical Specifications

Technical Specifications		
Printed Circuit Board	**Dimensions**	6U Eurocard (233x160mm^2), front panel width 20.3mm (4HP), mechanics constructed with respect to EMC requirements, ejector lever
CPU	**Microprocessor**	Intel i960RP/RD, 3.3V, 33/66MHz, clocked by system bus (local oscillator provided when operated as stand-alone)
	Memory	8MByte FPM/EDO DRAM, 32-bit, 4MByte FLASH ROM (SMT) 28F160S5 (Intel, Sharp), 32-bit
	Utilities	Watchdog and 5V/3.3V voltage-supervisor MAX705, serial EEPROM 4KByte I^{2}C, optional: ACCESS.bus interface
	Firmware	Mon960 Monitor/Debugger available
Serial Interfaces	**Interface Type**	asynchronous, serial protocol: 1 startbit; 7 or 8 databits; 1 or 2 stopbits; optional even/odd parity; standard bitrates up to 230.4 kbps
	Serial Interface Controller	16 x 16C550 asynchronous communication element, Texas Instruments TL16C550C or equivalent
	Physical Interface	UARTs 1-5 only: RS-232/V.24 by 75185 transceivers, all UARTs: TTL level signal additionally
	Connectors SP1-SP5	front panel mounted 9-pin D-Sub male connectors (RS-232E, PC compatible)
	Connectors J4/J5	TTL-level signals routed to the J4 and J5 connectors for arbitrary use with rear I/O transition board and PHY interface modules providing the external transceiver circuitry
	Drivers	serial drivers (COM port emulation) available for Windows NT4.0 and Windows 2000, others forthcoming
CompactPCI® Bus	**Connector J1**	32-Bit, 33MHz (133MBps) 32-Bit DMA Bus Master (133MBps) PCI Burst Mode 5V Interface
Power Supply	**Connector J1**	+5V ±5% 0.5A max. (without optional rear-I/O PHY transceiver modules) +3.3V ±0.3V 0.7A (i960RP) 0.9A (i960RD) max. +12V±5% 0.1A max. -12V±5% 0.1A max.
Temperature Humidity	**Commercial Grade Version**	operating temperature 0-70°C humidity 5-90% non condensing

Technical specifications are subject to change

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Rear-I/O Module

CU9-1-BASE Rear-I/O Transition Board with CU7/CU8 PHY Modules

The rear-I/O signals, derived from the CU1-CHORUS, are passed via its CPCI connectors J4/J5, across the backplane, to the additionally available transition board CU9-1-BASE. There are sixteen CU9-internal headers (H1..H16) provided on-board for attachment of up to 16 rear-I/O PHY interface modules of the CU7/CU8 series across micro-ribbon flat cables. The PHY interface modules can be directly mounted to the 6U/12HP back panel of the CU9-1-BASE transition board. In order to avoid possible signal conflicts, your CompactPCI system must be stuffed with a suitable P4/P5 backplane for rear-I/O (J4 on the CU1-CHORUS is coded with a brown key). A single slot P4/P5 backplane is available from EKF (see ordering information table).

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Ordering Information

Ordering Information		
Alias	Ordering No.	Short Description
CHORUS	CU1-1-CHORUS	6U, *CompactPCI* 16-port serial asynchronous interface subsystem with i960RP CPU/bridge, 4MB Flash, 8MB DRAM, MON960, 5 ports configured as RS-232 directly available from the front panel, all ports additionally routed across optional J4/J5 as TTL level signals for use with rear I/O transition board and PHY interface modules
	CU7-1-RS485	RS-485/RS-422 rear-I/O PHY interface module w/o galvanic isolation, including flat cable assembly
	CU7-2-RS485	RS-485/RS-422 rear-I/O PHY interface module with galvanic isolation, including flat cable assembly
	CU8-1-RS232	RS-232E/V.28 rear-I/O PHY interface module, including flat cable assembly
	CU9-1-BASE	Transition board, bridging function between CU1-CHORUS (J4/J5) and rear-I/O PHY interface modules, 16 ports, 6U/12HP back panel, be sure to order the CU1-CHORUS with built in J4/J5 connectors for rear-I/O
	932.2.01.000	Single slot P4/P5 rear-I/O backplane, suitable for CU1-CHORUS and CU9-BASE

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